

05/04/99
JC558 U.S. PTO

PATENT APPLICATION
Attorney's Do. No. 5484-48

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JC490 U.S. PTO
09/305240
05/04/99

EXPRESS MAIL MAILING LABEL NO. EL 089101263 US
DATE OF DEPOSIT: MAY 4, 1999
I HEREBY CERTIFY THAT THIS PAPER AND ENCLOSURES AND/OR FEE ARE BEING DEPOSITED
WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE"
SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO: BOX
PATENT APPLICATION, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON D.C. 20231.

JOANNA MOSSER *Joanna Mosser*
(SENDER'S PRINTED NAME) (SIGNATURE)

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor: **Byung-Sup SHIM et al.**

For: **OPEN DRAIN INPUT/OUTPUT STRUCTURE AND MANUFACTURING METHOD THEREOF
IN SEMICONDUCTOR DEVICE**

Enclosures:

- ☒ Specification (pages 1-8); claims (pages 9-10); abstract (page 11)
- ☒ 7 sheet(s) of formal drawings
- ☒ Executed Combined Declaration and Power of Attorney
- ☒ Korean Priority Document #98-15975, filed May 4, 1998
- ☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703

CLAIMS AS FILED				
For	Number Filed	Number Extra	Rate	Basic Fee \$760
Total Claims	-20		x \$ 18 =	
Independent Claims	-3		x \$ 76 =	
TOTAL FILING FEE				\$760

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM P.C.

Alan T. McCollom

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM P.C.
1030 S.W. Morrison Street Portland OR 97205 (503) 222-3613

OPEN DRAIN INPUT/OUTPUT STRUCTURE AND MANUFACTURING METHOD THEREOF IN SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and manufacturing method thereof, and more particularly to an open drain input/output structure and manufacturing method.

2. Description of the Prior Art

In general, when an input/output (I/O) of a MASKROM embedded MCU is implemented, it is necessary to establish a single layout for an open drain option and for a pull-up option. Accordingly, when devices in the MASKROM embedded MCU are manufactured, two I/Os (open drain I/O and pull-up I/O) are typically implemented as transistors, and more particularly as follows.

A pull-up I/O is first formed in such a manner that a contrary type of impurity to a substrate is ion-implanted into the channel region so that a gate is formed. Thereafter an open drain I/O is formed by starting with what would be a depletion transistor, and converting it into an enhancement transistor by further ion-implanting an impurity of the same type as the substrate into only a specific region. The specific region is the channel region of a cell which would be used as an open drain option during after gate programming (AGP) process.

The selective change of the depletion transistor into the enhancement transistor is for cutting off the depletion transistor for a pull-up resistance by the impurity ion implantation process (because a current flow occurs through the pull-up resistance, thereby causing an external component not to be controlled, when the both terminals of the pull-up resistance of the pull-up resistance type I/O are applied with an electric voltage source of a chip and an external high voltage). Here, the open drain I/O controls components by using an external high voltage.

That is, the depletion transistor is used as the pull-up resistance on the condition that the depletion transistor is changed into the enhancement transistor by the impurity ion implantation process for a channel region after being patterned a gate when the depletion transistor is intended to use as the open drain I/O.

FIG. 1 shows a circuit corresponding to a conventional open drain I/O structure. Reference numeral C represents a cutting-off node of the open drain circuit, D an open drain I/O input terminal, E an external component and Vdd an internal voltage terminal.

Two transistors A, B are respectively connected to a second and first internal logic circuits 10b and 10a. Transistor A is a n-channel open drain transistor. Transistor B is a pull-up or enhancement transistor, which has been so made by changing an n-channel depletion transistor by ion implanting impurities, after the gate is formed. The two transistors are connected in series each other through cutoff node C, which in turn is connected to an input/output pad 20. The pad 20 is connected with an external analog IC for applying an external high voltage unlike MOS-type LSI.

Pull-up transistor B is connected between a Vdd terminal and a pad 20 by the source and the drain. Because it should be maintained in the cut-off state, the first internal logic circuit 10a should be established to output a low level signal. When the second internal logic circuit 10b keeps a high level, an external signal is applied through the pad 20, and then a current flows through the open drain transistor A, so as to operate the external component.

FIG. 2 shows a conventional structure of a n-channel open drain transistor A. A gate insulating layer 34 is formed on an active region of a p-type semiconductor substrate 30 which is formed with a field oxide film 32.

A gate 26 is formed on a predetermined portion of the gate insulating layer 34. The gate is preferably formed with a layer of a W-silicide 26b accumulated on a polysilicon layer 26a.

An insulative spacer 28 is formed on each side wall of the gate 26. N-type source and drain regions 42a and 42b are formed in substrate 30, provided with LDD (lightly doped drain) regions 40. A channel region is defined between them.

Referring to FIG.s 3 and 4, an enhancement transistor B is shown. It has a very similar structure to transistor A of FIG. 2, except for the following. The gate is numbered 36, is comprised of respective layers 36a, 36b, and its line width is W2. Spacers 38 are formed around it.

Further, at the channel region under gate 36, a n-type impurity implantation region 44 is formed. It is over a region that is adjacent to or even overlaps both the source and drain, and thus forms a continuous path of a n-type impurity between them.

Additionally, a p-type impurity implantation region 46 is further formed at a middle section of region 44. The p-type impurity implantation region serves as the pull-up resistance

after the gate is formed. This ensures that a constant off state is kept, except when the gate is provided with a high level signal.

The conventional method for forming the open drain I/O has the following drawbacks: First, in transistor B, the additional impurity ion implantation process must be performed one more time for forming the p-type impurity implantation region 46, after the gate is formed. This causes not only the process to be complicated, but also cost to be increased.

Second, when a system maker intends to achieve a EPROM embedded MCU by using a non-volatile memory (for example EPROM for the purpose of developing a program and for applying to the market), there is no problem to achieve the open drain I/O by the process and the layout different from a conventional mask ROM embedded MCU. However, there is a problem for the open drain I/O to achieve by using the same layout as the conventional layout. That is, since an AGP (after gate programming) coding is not used for the EPROM embedded MCU, it is not necessary the impurity ion implantation process after the gate is formed. Therefore, it is not possible to achieve selectively between the I/O for the pull-up resistance of the EPROM embedded MCU and the open drain I/O. That is, it is possible for the mask ROM embedded MCU to achieve the open drain I/O and the I/O for pull-up resistance, but it is possible for the EPROM embedded MCU to achieve only the I/O for pull-up resistance.

Therefore, it is required for the open drain I/O having the same layout to apply in the mask ROM embedded MCU and the EPROM embedded MCU.

SUMMARY OF THE INVENTION

The present invention overcomes these problems of the prior art. The invention provides an improved pull-up transistor that is to be used in place of the enhancement transistor B of the prior art. The transistor includes a source and a drain that can be connected to a Vdd terminal and to an I/O pad. In the channel of the transistor there is an impurity implantation region that does not reach both the source and the drain. In other words, it presents a discontinuity, which serves as a p-type channel. This avoids the need of the prior art for the additional p-type ion-implantation process, after forming the gate.

According to the first embodiment, the impurity reaches the source, but not the drain. In the second embodiment, the impurity reaches the drain, but not the source. In the third embodiment the impurity reaches neither the source nor the drain, thus presenting at least two

discontinuities. The invention can be implemented with a mask ROM embedded MCU, an EPROM embedded MCU.

Another object of the present invention is to provide an open drain input/output transistor manufacturing method, which enables to effectively achieve an open drain structure of the input/output.

The invention also provides a method of manufacture of the device. A gate insulating layer is formed in an active region on a p-type semiconductor substrate; then an impurity implantation region is formed at a predetermined first sector within the substrate by ion-implanting a n-type impurity. Then a gate is formed on the gate insulating layer over at least a portion of the first sector and over a region adjacent to the first sector. Source and drain regions are then formed within the substrate at opposite sides of the gate, by ion-implanting an impurity of the second conductive type. The first sector having been predetermined such that it does not reach both the source region and the drain region.

As a result, using the open drain I/O of the invention enables implementing a MASKROM embedded MCU, I/O for pull-up resistance of EPROM embedded MCU, and open drain I/O with a single lay out structure, which makes it compatible for manufacture with MCU, and more economical.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object, and other features and advantages of the present invention will become apparent after a reading of the following detailed description when taken in conjunction with the drawings, in which:

FIG. 1 is a schematic circuit diagram illustrating an open drain input/output stage structure of a conventional semiconductor device;

FIG. 2 is a sectional view of open drain transistor A in FIG. 1;

FIG. 3 is a sectional view of pull-up transistor B in FIG. 1;

FIG. 4 is a plan view illustrating the layout structure after the gate is formed in the transistor of FIG. 3;

FIGS. 5a to FIG. 5c are views illustrating an input/output stage structure of a semiconductor device made according to the first embodiment of the present invention, and more specifically:

FIG. 5a is a sectional view illustrating the enhancement transistor structure of the open drain input/output stage,

FIG. 5b is a plan view illustrating the layout structure after the gate is formed, and

FIG. 5c is an equivalent circuit of FIG. 5a;

FIG. 6a to FIG. 6c are views illustrating an input/output stage structure of a semiconductor device made according to the second embodiment of the present invention, and more specifically:

FIG. 6a is a sectional view illustrating the enhancement transistor structure of the open drain input/output stage,

FIG. 6b is a plan view illustrating the layout structure after the gate is formed, and

FIG. 6c is an equivalent circuit of FIG. 6a;

FIG. 7a to FIG. 7c are views illustrating an input/output stage structure of a semiconductor device made according to the third embodiment of the present invention, and more specifically:

FIG. 7a is a sectional view illustrating the enhancement transistor structure of the open drain input/output stage,

FIG. 7b is a plan view illustrating the layout structure after the gate is formed, and

FIG. 7c is an equivalent circuit of FIG. 7a.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As has been mentioned, the present invention is directed to an improved pull-up transistor that is to be used in place of the enhancement transistor B of FIG. 1 of the prior art. The transistor includes a source and a drain that can be connected to a Vdd terminal and to an I/O pad. In the channel of the transistor there is an impurity implantation region that does not reach both the source and the drain.

In the following description, the line width F of the active region becomes important, along with the line widths of the impurity implantation region and of the gate. But for the special impurity implantation region, the transistor would be a n-channel open drain transistor, whose separate description is thus omitted.

Embodiment 1

The first embodiment H1 is now described with reference to FIG.s 5a, 5b and 5c. As shown in FIG. 5a, a gate insulating layer 34 with a field oxide layer 32 is formed at an active region of a p-type semiconductor substrate 30. N-type source and drain regions 42a and 42b are formed, defining between them a channel region. They are optionally provided with LDD regions 40.

A n-type impurity implantation region 54 is formed at a first sector of the channel region. While it is coupled to source region 42a, but maintains a predetermined distance -o- from drain region 42b, which is different than in the prior art.

A gate 56 is formed on the gate insulating layer 34. What is further different is that gate 56 is formed on a predetermined portion of the gate insulating layer. Specifically, W3 indicates the line width of gate 56, and F indicates the line width of the active region. The gate is formed over a first portion of the first sector and over a portion of the area adjacent the first sector.

The gate is formed by accumulating a polysilicon layer 56a and a W-silicide (W-silicide/ polysilicon) layer 56b. Other embodiments are possible, such as a one step polysilicon layer. Then both side walls are formed with an insulating spacer 58.

The enhancement transistor H1 having the above-structure is manufactured through the following four steps.

As a first step, the gate insulating layer 34 is formed at the active region on the p-type semiconductor substrate 30, which is formed with the field oxide layer 32. Then an n-type impurity is selectively implanted on a selected portion of the gate insulating layer 34. Accordingly, an n-type impurity implantation region 54 is formed at the portions in the substrate 30, which are collectively known as the first sector of the substrate.

As a second step, the gate 56 is formed on the gate insulating layer 34. The gate is over a first portion of the first sector, i.e. over at least some of the impurity implantation region 54. The gate is also over a second portion of the surface of the substrate 30 that is adjacent region 54. The gate can be manufactured by depositing a conductive layer and then selectively etching it to conform to the desired shape.

Because the n-type impurity implantation region 54 should be formed only at the certain portions of the channel region in order to achieve the open drain structure without the p-type impurity ion implantation process for opening the channel, the gate 56 should be formed to have a little longer length W3 than the conventional length W2 of FIG. 2. This is best seen with reference to FIG. 5b.

As a third step, the n-type impurity in low concentration is ion-implanted to the substrate 30 through the gate 56, as a mask so as to form LDD regions 40 in the substrate 30 at both sides of the gate.

As a fourth step, insulating spacers 58 are formed at both side walls of the gate 56. Then the n-type impurity in high concentration is ion-implanted to the substrate 30, using the

gate and the spacer 38 as a mask, so as to form the source/drain regions 42a and 42b in the substrate 30.

FIG. 5c illustrates the operation of transistor H1. Transistor H1 operates as a depletion transistor HD in the first sector, which is where the n-channel region includes the n-type impurity implantation region 54. However, it operates as an enhancement transistor HE at the region adjacent the first sector, i.e. the p-channel region (portion "O" in drawing) where the channel lacks the impurity implantation region 54. Accordingly, the enhancement transistor can be cut-off only when a voltage Vdd is applied to the source region, and a low level signal is applied to the gate.

Embodiment 2

The second embodiment H2 is now described with reference to FIG. 6a, 6b and 6c. It is the same as the first embodiment, except that the first sector reaches the drain region instead of the source region. In other words, a n-type impurity implantation region 64 is formed contiguously to, or overlapping with the drain region, but maintains a predetermined distance -o- from a source region.

FIG. 6c shows an equivalent circuit for transistor H2 of FIG. 6a. Transistor H2 operates similarly to transistor H1 of FIG. 5c.

Embodiment 3

The third embodiment H3 is now described with reference to FIG. 7a, 7b and 7c. It is the same as the first two embodiments, except that the first sector does not reach either one of the source and drain regions. More specifically, a n-type impurity implantation region 74 is formed at predetermined distances from source/drain regions 42a, 42b. Preferably the predetermined distances are equal.

The enhancement transistor having the above-structure is manufactured through substantially the same steps, taking care that the n-type impurity implantation region 74 is formed at portions of the substrate that do not overlap or even contact the source and drain. Further, the gate 56 is formed on the gate insulating layer 34 so as to be over a first portion of the first sector and over a second portion of the surface of the substrate 30 adjacent the first sector. Preferably the first portion is in a predetermined ratio with the second portion.

FIG. 7c shows an equivalent circuit for the transistor in FIG. 7a. P-channels (parts "o" in the drawing) are formed at both sides of the n-channel region, adjacent to the impurity implantation region 44. Transistor H3 having the above structure operates at the p-channel

regions as enhancement transistors HE, HE', and operates at the n-channel regions as depletion transistor HD. Therefore, transistors HE, HE' can be cut off only when a low level signal is applied to the gate, with the voltage Vdd being applied to the source region.

A person skilled in the art will be able to practice the present invention in view of the present description, where numerous details have been set forth in order to provide a more thorough understanding of the invention. In other instances, well-known features have not been described in detail in order not to obscure unnecessarily the invention.

Having illustrated and described the principles of the invention in its preferred embodiments, it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. For example, the conductivity types (p-type and n-type, also collectively known as conductive types) can be interchanged. All modifications coming within the spirit and scope of the accompanying claims are claimed as follows.

WHAT IS CLAIMED IS:

1. A method of manufacturing a pull-up transistor for use with a Vdd terminal and an I/O pad of a semiconductor device comprising:

5 forming a gate insulating layer in an active region on a first conductive-type semiconductor substrate;

forming an impurity implantation region at a predetermined first sector within the substrate by ion-implanting an impurity of a second conductive-type;

10 forming a gate on the gate insulating layer over at least a portion of the first sector and over a region adjacent to the first sector;

forming source and drain regions within the substrate at opposite sides of the gate by ion-implanting an impurity of the second conductive type, the first sector having been predetermined such that the impurity implantation region does not reach both the source region and the drain region;

15 coupling one of the source region and the drain region to the I/O pad; and

coupling the other one of the source region and the drain region to the Vdd terminal.

2. The method of claim 1, wherein the gate is formed by depositing a conductive layer and then selectively etching it.

20 3. The method of claim 1, wherein forming the impurity implantation region is by ion-implanting at a low concentration.

4. The method of claim 1, further comprising:

25 forming LDD regions at both sides of the gate; and

forming a spacer adjacent the gate before forming the source and drain regions.

5. A pull-up transistor for use with a Vdd terminal and an I/O pad of a semiconductor device comprising:

30 a semiconductor substrate of a first conductive-type;

a source region and a drain region of a second conductive type formed in the substrate and defining between them a channel region, one of the source region and the drain region being coupled with the I/O pad, the other one of the source region and the drain region being coupled with the Vdd terminal;

an impurity implantation region of impurities of a second conductive-type formed in a first sector of the channel region, the first sector reaching at most one of the source region and the drain region;

a gate insulating layer on the substrate over at least a portion of the impurity implantation region and over at least a portion of an area adjacent the impurity implantation region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of a region adjacent to the first sector.

6. The transistor of claim 5, wherein the first sector has a narrower line width than a line width of the gate.

7. The transistor of claim 5, wherein the gate is over a first portion of the first sector and over a second portion of an area adjacent the first sector, and wherein the first portion is in a predetermined ratio with the second portion.

8. The transistor of claim 5, wherein the first sector does not reach either one of the source region and the drain region.

9. The transistor of claim 8, wherein the first sector is separated from the source region and from the drain region by equal distances.

OPEN DRAIN INPUT/OUTPUT STRUCTURE AND MANUFACTURING METHOD THEREOF IN SEMICONDUCTOR DEVICE

ABSTRACT

5 An improved pull-up transistor is provided for use as an open drain input/output
structure. The transistor includes a source and a drain that define a channel between them.
An impurity implantation region in the channel does not reach both the source and the drain.
The impurity can reach only the source, only the drain, or none of them. As such, it presents a
discontinuity, which serves as a p-type channel. The transistor therefore can act as an
10 enhancement transistor used for pull-up. The invention can be implemented with a mask
ROM embedded MCU, or an EPROM embedded MCU.

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2

FIG.1(Prior Art)

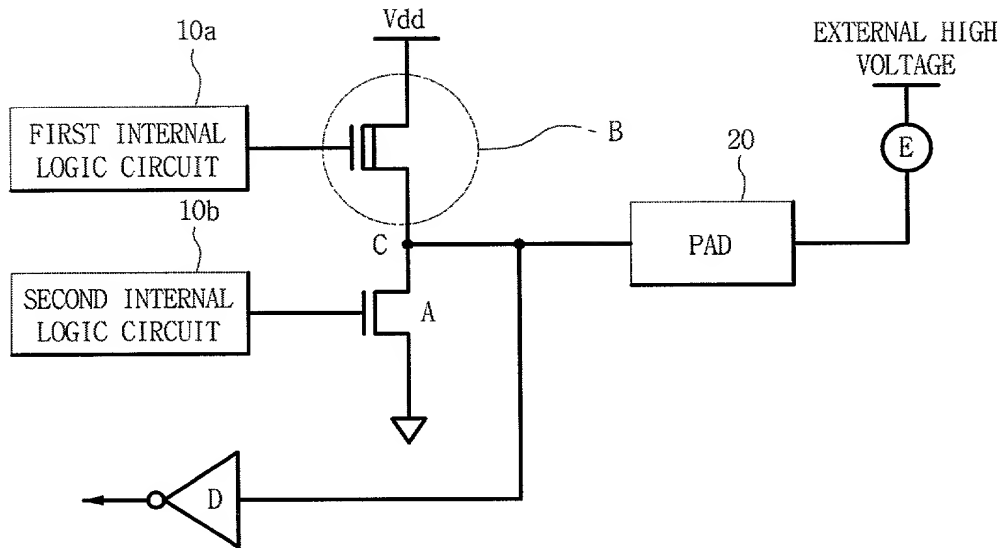
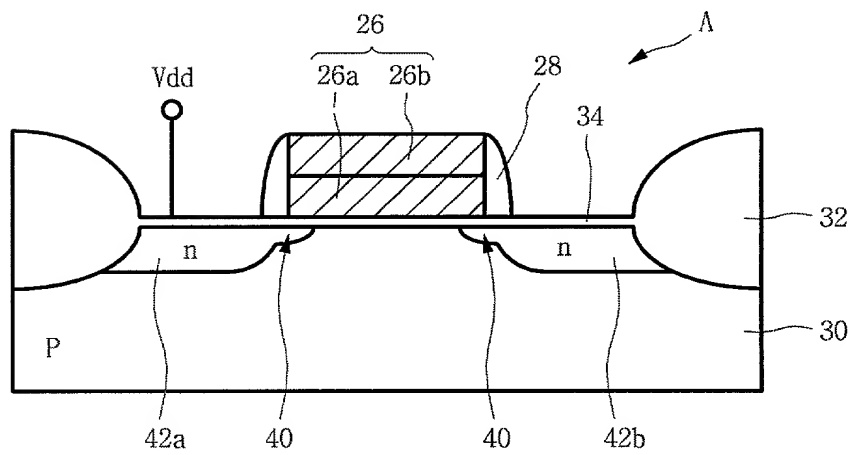
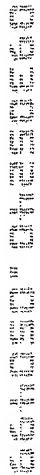
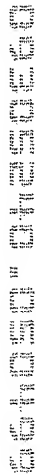


FIG.2(Prior Art)



[illegible][illegible]

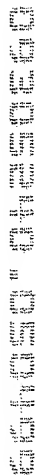
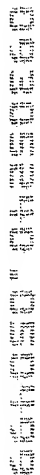
[illegible][illegible]

FIG. 6b

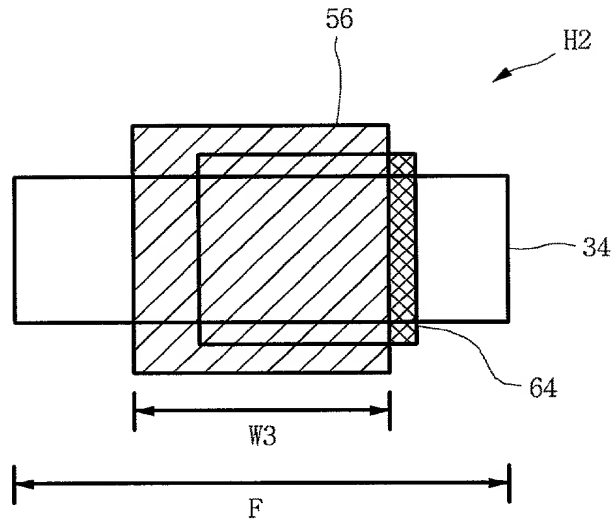
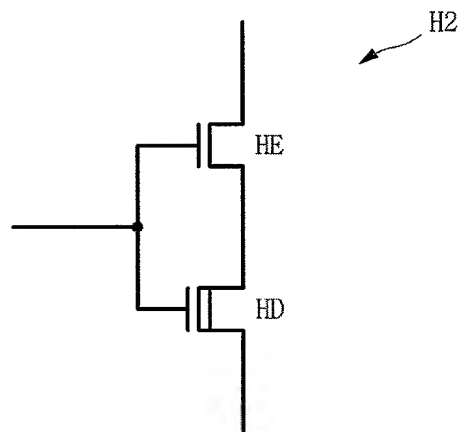


FIG. 6c



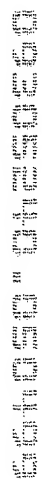
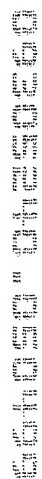
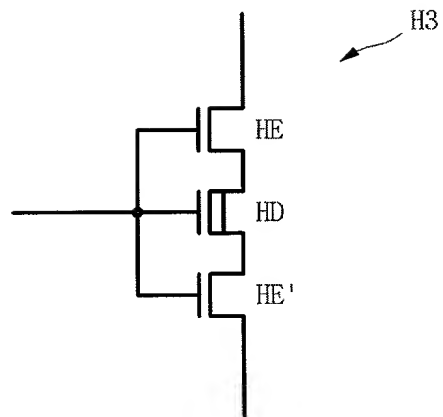
[illegible][illegible]

FIG.7c



PATENT APPLICATION
Attorney Docket No. 5484-48

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
, the specification of which:

☒ is attached hereto.
☐ was filed on _____ as Application No. _____
☐ and was amended on _____ (if applicable)
☐ with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
<u>98-15975</u>	<u>Korea</u>	<u>4 May 1998</u>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.

Filing Date

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

<u>(Application No.)</u>	<u>(Filing Date)</u>	<u>(Status) (patented, pending, abandoned)</u>
--------------------------	----------------------	--

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Customer No. 20575

<u>Attorney Name</u>	<u>Registration No.</u>
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
Glenn C. Brown	34,555
Stephen S. Ford	35,139
Gregory T. Kavounas	37,862
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Vernon W. Francissen	41,762
Graciela G. Cowger	42,444
Ariel Rogson	43,054

Direct all telephone calls to at (503) 222-3613 and send all correspondence to:

MARGER JOHNSON & MCCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: **Byung-Sup SHIM**

Inventor's signature: Byung Sup Shim

April/23/99
(Date)

Residence: Korea

Citizenship: Korea

Post Office address: #307-803, Chugong 3 danji, Chang 1-dong, Dobong-ku,
Seoul, Rep. of Korea

Full name of second joint inventor: **Young-Ho KIM**

Inventor's signature: Young Ho Kim

April/23/99
(Date)

Residence: Korea

Citizenship: Korea

Post Office address: #102-508, Punglim Apt., Kugal-ri, Kiheung-eup, Yongin-city,
Kyungki-do, Rep. of Korea